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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/612,281 | 06/30/2003 | Brian Taggart | 884.853US1 | 5797 |

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| EXAMINER | |
|---|---|
| NORRIS, JEREMY C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2841 | |

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/612,281 | TAGGART ET AL. | |
| | Examiner | Art Unit | |
| | Jeremy C. Norris | 2841 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

The claims are objected to because they include reference characters which are not enclosed within parentheses (see particularly claim 7).

Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5, 8, 9, 14, and 17-23 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,365,433 (Hyoudo).

Hyoudo discloses, referring primarily to figures 2A-B, an article comprising: a wire-bonding mounting substrate (21) including a first surface and a second surface; a first wire-bond pad (27) disposed upon the first surface; and a first via (35) in the wire-

bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad [claim 1], wherein the via includes a liner (see col. 3, lines 5-25) that is electrically conductive [claim 3], further including an interconnect filling the via (see col. 3, lines 5-25) [claim 4] wherein the via includes a liner (22A), further an interconnect filling the via (see col. 3, lines 5-25) [claim 5].

Additionally, Hyoudo discloses, a package comprising: a wire-bonding mounting substrate (21) including a first surface and a second surface; a first wire-bond pad (27) disposed upon the first surface; a first via (35) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad (fig. 2B); a die (29) disposed on the first surface and a first wire bond (30) that couples the die to the first wire-bond pad [claim 8], further including a second wire-bond pad (28) disposed upon the first surface a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad [claim 9], wherein the first wire-bond pad is part of a plurality of wire-bond pads (27, 28), and wherein each wire-bond pad is directly above a corresponding via from a plurality of vias [claim 14].

Moreover, Hyoudo discloses, referring to figures 2A-B, a process comprising: forming a first via (35) in a wire-bonding mounting substrate (21), wherein the wire-bonding mounting substrate includes a first surface and a second surface, and wherein forming proceeds from the second surface toward the first surface; and patterning a first

wire-bond pad (27) symmetrically and directly over the first via [claim 17] wherein forming ceases upon contact with the first wire-bond pad [claim 18], further including forming a via liner (col. 3, lines 5-25) in the first via [claim 19], further including: filling the first via with an interconnect (col. 3, lines 5-25) [claim 20], wherein forming the first via precedes patterning the first wire-bond pad (fig. 2A-2E) [claim 21], further including: filling the first via with an interconnect; coupling the first via to a first bump (36) [claim 22], further including: coupling the first wire-bond pad to a first bump (36) [claim 23].

Claims 2, 8, 9, 11, 12, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,084,295 (Horiuchi).

Horiuchi discloses, referring primarily to figures 4 and 5, an article comprising: a wire-bonding mounting substrate (5) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; and a first via (18) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed directly below the first wire-bond pad, wherein the wire-bonding mounting substrate includes a first edge, the article further including: a second wire-bond pad disposed upon the first surface; a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad; and wherein the first via and the second via are staggered with respect to the first edge of the wire-bonding mounting substrate (see figure 4) [claim 2].

Similarly, Horiuchi discloses, a package comprising: a wire-bonding mounting substrate (5) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; a first via (18) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed symmetrically and directly below the first wire-bond pad; a die (10) disposed on the first surface and a first wire bond (20) that couples the die to the first wire-bond pad [claim 8], further including: a second wire-bond pad disposed upon the first surface; a second via in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad (see figure 5) [claim 9], further including: a first bump (12) coupled to the first via [claim 11], further including: a first bump (12) coupled to the first via; and a first trace (24) that makes an electrical contact to the first bump [claim 12], wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, and wherein each via is coupled to a bump [claim 15], wherein the first wire-bond pad is part of a plurality of wire-bond pads, wherein each wire-bond pad is directly above a corresponding via from a plurality of vias, wherein each via is coupled to a bump (12), and wherein each bump is directly below a corresponding via (see figure 5) [claim 16].

Claims 24-27 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,784,376 (Huemoeller).

Huemoeller discloses, a method comprising: forming a first via in a wire-bonding mounting substrate (20), wherein the wire-bonding mounting substrate includes a first surface and a second surface, and wherein forming proceeds from the second surface toward the first surface, patterning a first wire-bond pad (22A) directly over the first via; and coupling a die (31) to the first wire-bond pad [claim 24], further including: forming a second via in the wire-bonding mounting substrate (col. 3, lines 10-25); patterning a second wire-bond pad directly over the second via; and coupling the die to the second wire-bond pad (col. 3, lines 10-25) [claim 25], further including: filling the first via with an interconnect [claim 26], further including: filling the first via with an interconnect; and coupling the first via to a first bump (36) [claim 27].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hyoudo in view of Huemoeller.

Hyoudo discloses the claimed invention as described above except Hyoudo does not specifically state wherein the wire-bond pad includes a first layer and a second layer, wherein at least one of the first layer and the second layer is selected from a precious metal, a precious metal alloy, silver, gold, platinum, nickel, palladium, platinum, cobalt, rhodium, iridium, and combinations thereof [claim 6] wherein the wire-bond pad includes a first layer and second layer, and wherein the second layer is one of identical material to the first layer, or at least one of a more noble or a softer metal than the first layer [claim 7]. However, Huemoller teaches a wire-bond pad which includes a first layer and a second layer (22, 23), wherein at least one of the first layer and the second layer is selected from a precious metal, a precious metal alloy, silver, gold, platinum, nickel, palladium, platinum, cobalt, rhodium, iridium, and combinations thereof (col. 3, lines 10-25), wherein the wire-bond pad includes a first layer and second layer, and wherein the second layer is one of identical material to the first layer, or at least one of a more noble or a softer metal than the first layer (col. 2, line 60 – col. 3, line 10) [claim 7]. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use the multilayer wire bond pad taught by Huemoller in the invention of Hyoudo. The motivation for doing so would have been to use a wire bond pad with

proper electrical conduction properties which is resistant to oxidation (see Huemoller col. 3, lines 1-10). Moreover, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin,* 125 USPQ 416.

Claims 8, 10 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,812,580 (hereafter Wenzel) in view of Hyoudo.

Wenzel discloses, referring to figure 2, a package comprising: a wire-bonding mounting substrate (11) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; a first via (72) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed directly below the first wire-bond pad; a die (12) disposed on the first surface and a first wire bond (60) that couples the die to the first wire-bond pad. Wenzel does not specifically state that the via is symmetrically below the pad [claim 8]. However, Hyoudo teaches locating vias directly and symmetrically below wire bond pads (see figure 2B). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to locate the vias symmetrically and directly below the wire bond pads in the invention of Wenzel as taught by Hyoudo. The motivation for doing so would have been to provide regular spacing between the vias to be used for signal routing. Moreover, it has been held that more than a mere change of form is necessary for patentability. Span-Deck, Inc v. Fab-con, Inc. (CA 8, 1982) 215 USPQ 835.

Additionally, the modified invention of Wenzel teaches, further including: a second wire-bond pad (14) disposed upon the first surface; a second via (70) in the wire-bonding mounting substrate, wherein the second via is in electrical contact with the second wire-bond pad, and wherein the second via is disposed directly below the second wire-bond pad; a second bond wire (61) that couples the die to the second wire-bond pad; and wherein the respective lengths of the first bond wire and the second bond wire are adjusted so as to tune the package (col. 2, lines 1-25) [claim 10].

Similarlay, Wenzel discloses, a computing system comprising: a wire-bonding mounting substrate (11) including a first surface and a second surface; a first wire-bond pad (22) disposed upon the first surface; a first via (72) in the wire-bonding mounting substrate, wherein the first via is in electrical contact with the first wire-bond pad, and wherein the first via is disposed directly below the first wire-bond pad; a die (12) disposed on the first surface; and DRAM coupled to the die (see col. 13, lines 1-10). Wenzel does not specifically state that the via is symmetrically below the pad [claim 28]. However, Hyoudo teaches locating vias directly and symmetrically below wire bond pads (see figure 2B). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to locate the vias symmetrically and directly below the wire bond pads in the invention of Wenzel as taught by Hyoudo. The motivation for doing so would have been to provide regular spacing between the vias to be used for signal routing. Moreover, it has been held that more than a mere change of form is necessary for patentability. Span-Deck, Inc v. Fab-con, Inc. (CA 8, 1982) 215 USPQ 835.

Furthermore, the modified invention of Wenzel teaches wherein the computing system is disposed in one of a computer, a. wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft (col. 13, lines 1-5) [claim 29], wherein the die is selected from a data storage device, a digital signal processor, a micro controller, an application specific integrated circuit, and a microprocessor (col. 13, lines 1-5) [claim 30].

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi in view of US 2003/0147227 A1 (Egitto).

Horiuchi discloses the claimed invention as described above except Horiuchi does not specifically state that the first bump (12) is coupled to the first via (18); and a larger substrate coupled to the first bump. However it is well known in the art to attach a semiconductor device to a larger substrate as evidenced by Egitto (figure 1). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to couple the bump in the invention of Horiuchi to a larger substrate as is well known in the art and evidenced by Horiuchi. The motivation for doing so would have been to allow for the sharing of signals between several devices.

### *Response to Arguments*

Applicant's arguments with respect to claims 1-23 and 28-30 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 2 May 2005, regarding claims 24-27 have been fully considered but they are not persuasive. Applicants allege that the claims have been amended to include the limitation that the via must be symmetrically disposed below the pad. However, no such amendment has been made. Thus, Applicants base the patentability of claims 24-27 on a limitation that does not exist in those claims. Hence, the argument is unpersuasive.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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